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## **DIGITALLY CONTROLLED ANALOG RF FILTERING IN SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE**

This application claims the priority under 35 USC 119(e)(1) of the following  
5 copending U.S. provisional applications: 60/286,421, 60/286,564, 60/286,736, 60/286,787,  
and 60/286,788, all filed on April 25, 2001; 60/343,673 filed on December 28, 2001; and  
60/276,716 and 60/276,727, both filed on March 16, 2001. All of the aforementioned  
provisional applications are incorporated herein by reference.

### **FIELD OF THE INVENTION**

10 The invention relates generally to communication receivers and, more particularly, to  
subsampling receiver architectures.

### **BACKGROUND OF THE INVENTION**

A recent trend in direct-conversion receivers is to use subsampling. The basic  
approach is to sample the RF signal at an integer fraction of the carrier frequency greater  
15 than twice the bandwidth of the modulating signal. Spectral images of the modulating  
signals are repeated and down-conversion can be achieved by a low pass filter.

A general scheme based on subsampling operation is presented in D. H. Shen *et al.*,  
"A 900-MHz RF front-end with integrated discrete-time filtering," *IEEE JSSC*, Vol. 31, pp.  
1945-1954, Dec. 1996 (hereinafter Shen), and is shown in FIGURE 1. The RF input is  
20 sampled-and-held and followed directly by discrete time analog signal processing. The

baseband signal is converted using an A/D converter. Sampling the carrier frequency  $f_c$  at a rate  $f_s$  results in spectral images located at  $nf_s \pm f_c$  where  $n$  is an integer. A desired spectral image can be filtered using a discrete time analog filter. In this approach, the lowest power solution would involve a tradeoff analysis between the input rate of the A/D converter and the complexity of anti-aliasing filters (see Shen) by appropriate selection of  $f_s$  in relation with  $f_c$ . In this approach, channel select filtering, demodulation and baseband processing are done in the digital domain following the A/D converter. The final stages of the multi-stage analog filters can also be used to reduce the adjacent channel interferers, thereby reducing the dynamic range requirement and power dissipation of the A/D converter.

10 E. Cijvat *et al*, "A 1.8 GHz subsampling CMOS downconversion circuit for integrated radio applications," *ISCAS* 1998, Vol. 3, pp. 149-152, discloses a subsampling mixer implemented for 1.8 GHz RF system. The mixer is implemented using a track-and-hold circuit. A differential OTA is used to transfer the sampled charge to the output in order to cancel the charge feed-through and to attain high linearity. The speed of OTA determines  
15 the maximum  $f_s$ .

Another example of the subsampling approach is disclosed in A. Rofourgaran *et al.*, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1  $\mu$ m CMOS. II. Receiver design," *IEEE JSSC*, Vol. 33, pp. 535-547, April 1998, for a short-distance wireless binary FSK transceiver at 900 MHz. This approach substantially reduces power dissipation by  
20 hard-limiting the filtered output of a subsampling mixer. The high frequency images are rejected by -60 dB using a switched capacitor analog filter. The limiter serves to act as a 1-bit A/D converter which provides an over-sampled down-converted baseband signal. The

signal is decoded using a 1-bit FSK demodulator. The AGC functionality is achieved using the filter, limiter and demodulator. This structure is simpler than the general architecture that typically requires a multibit A/D converter and VGAs, and thereby saves power. However, its application is not directly extendable to general modulation schemes.

5           Conventional subsampling receiver designs eliminate the need for IF filters, image-reject mixers, image reject filters and analog I/Q branches, thereby permitting a high level of integration. Further, the LO (local oscillator) in such designs operates at a much lower frequency than  $f_c$ . However, this design trades one set of problems for another. Exemplary disadvantages in such receivers typically include sensitivity to clock jitter and poor linearity.

10           Conventional receivers based on the subsampling principle require sample-and-hold (S/H) or track-and-hold stages operating at the IF rate. The signal-to-noise ration of such stages are limited by the clock jitter and settling time requirement of the S/H. Such stages cannot practically operate at RF frequencies because the required power dissipation will be prohibitively large for the required dynamic range performance (dictating quick settling  
15           time) and sampling frequency (dictating frequency aliasing).

It is therefore desirable to provide a subsampling receiver architecture that avoids problems such as those mentioned above with respect to the prior art.

A subsampling receiver architecture according to the invention can advantageously avoid problems such as mentioned above in the downconversion of a first periodic voltage  
20           waveform into a second periodic voltage waveform. A plurality of temporally distinct samples respectively indicative of areas under corresponding half-cycles of the first voltage waveform are obtained, and the samples are combined to produce the second voltage

waveform. According to exemplary embodiments of the invention, the samples can also be manipulated to implement a filtering operation such that the second voltage waveform represents a downconverted, filtered version of the first voltage waveform.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 diagrammatically illustrates an example of a conventional subsampling receiver architecture.

FIGURE 2 diagrammatically illustrates pertinent portions of exemplary embodiments of a multi-tap digital subsampling receiver architecture according to the invention.

FIGURES 3 and 3A diagrammatically illustrate exemplary embodiments of portions of the multi-tap digital subsampling receiver architecture of FIGURE 2.

FIGURE 4 graphically illustrates exemplary signals of FIGURES 2 and 3.

FIGURES 5 and 5A illustrate in tabular format examples of how the digital control unit of FIGURE 3 can control the switches of FIGURE 3.

FIGURES 6 and 6A illustrate in tabular format further examples of how the digital control unit of FIGURE 3 can control the switches of FIGURE 3.

FIGURE 7 diagrammatically illustrates a general example of an FIR filter which can be implemented by the embodiments of FIGURE 3.

FIGURES 8 and 8A illustrate in tabular format examples of how the digital control unit of FIGURE 3 can control the switches of FIGURE 3 to implement desired FIR filter functions.

FIGURE 8B diagrammatically illustrates exemplary embodiments of the invention generally similar to those of FIGURE 3 but with added components for realizing triangular filter coefficients.

FIGURE 9, taken in conjunction with FIGURE 3, diagrammatically illustrates exemplary dummy sampler embodiments according to the invention.

FIGURE 10 diagrammatically illustrates exemplary embodiments of the invention wherein each capacitor of FIGURE 3 is replaced by a bank of capacitors.

FIGURE 11 diagrammatically illustrates exemplary embodiments of the capacitor banks of FIGURE 10.

5        FIGURE 12 illustrates in tabular format an example of how the digital control unit of FIGURE 11 can control the switches of FIGURE 11 to implement a desired FIR filter function.

FIGURE 13 diagrammatically illustrates further exemplary embodiments of the banks of FIGURE 10.

10        FIGURE 14 illustrates exemplary operations which can be performed by the embodiments of FIGURES 2-13.

FIGURE 15 illustrates how FIGURES 15A and 15B are to be viewed together.

FIGURES 15A and 15B illustrate in tabular format exemplary operations which can be performed by the architecture of FIGURE 3.

15        FIGURE 16 diagrammatically illustrates exemplary embodiments of the invention which permit resetting the IF amplifier of FIGURE 3.

FIGURE 17 illustrates how FIGURES 17A and 17B are to be viewed together.

FIGURES 17A and 17B illustrate in tabular format exemplary operations which can be performed by the embodiments of FIGURE 16.

20        FIGURE 18 illustrates in tabular format exemplary operations which can be performed by the embodiments of FIGURE 3.

FIGURE 19 is a timing diagram which illustrates exemplary operations which can be performed by the embodiments of FIGURE 3.

FIGURE 20 diagrammatically illustrates a differential filter which can be implemented by the embodiments of FIGURES 2-13.

5        FIGURES 21 and 22 illustrate exemplary positioning of a recursive FIR filter for cooperation with the differential filter of FIGURE 20.

FIGURE 23 diagrammatically illustrates further exemplary embodiments of portions of the architecture of FIGURE 2.

10        FIGURE 24 illustrates in tabular format exemplary operations which can be performed by the embodiments of FIGURE 23.

FIGURE 25 diagrammatically illustrates an equivalent filter produced by the operations of FIGURE 24.

FIGURE 26 diagrammatically illustrates exemplary embodiments of the invention that can perform I/Q mixing.

15        FIGURE 27 graphically illustrates exemplary control signals which can be used in the embodiments of FIGURE 26.

## DETAILED DESCRIPTION

FIGURE 2 diagrammatically illustrates pertinent portions of exemplary embodiments of a subsampling communication receiver according to the invention. The subsampling receiver architecture of FIGURE 2 includes an input 20 for receiving the voltage waveform of a communications signal, for example an RF communication signal. This voltage waveform is applied to a low noise transconductance amplifier (LNTA) 22 which can use conventional techniques to transform the voltage waveform at 20 into a corresponding current waveform at 21. In some embodiments, the LNTA 22 can include a conventional low-noise amplifier (LNA) followed by a conventional transconductance amplifier (TA). The current waveform at 21 is applied to a switch and capacitor network 23. Switches in the network 23 are operable for sampling the current waveform, and capacitors in the network 23 are operable for integrating the current waveform samples. A digital control unit (DCU) controls the operation of the switches in the switch and capacitor network 23. At 29, the DCU receives oscillator signals from a local oscillator (LO). The switch and capacitor network 23 has an output for providing the aforementioned integrated current samples to an IF (intermediate frequency) amplifier 25 (also referred to as IFA) whose output drives an analog signal processing section 26, which in turn drives an A/D converter 27. The digital baseband signal output from the A/D converter 27 is passed on to a baseband processing portion of the receiver.

FIGURE 3 diagrammatically illustrates exemplary embodiments of pertinent portions of the receiver of FIGURE 2, which portions operate to mix the input signal from a higher to lower frequency, for example, from RF to IF. In particular, FIGURE 3 illustrates the LNTA



22 coupled at 21 to the switch and capacitor network 23. FIGURE 3 also illustrates an exemplary DCU 34 which controls various switches (e.g., transistor switches) in the network 23 via control busses 31, 32 and 33. The switch and capacitor network 23 includes outputs which are respectively coupled to the non-inverting and inverting inputs 35 and 36 of the IF amplifier 25. The LNTA 22 (e.g. a linear LNTA) and the IF amplifier 25 can be implemented, for example, with conventionally available designs. In some embodiments, the LNTA replaces the LNA of conventional designs. In other embodiments, an LNA with a gain greater than 1 is provided upstream of the LNTA.

The switch and capacitor network 23 includes a plurality of stages (eight in the example of FIGURE 3), each of which includes a sampling switch S, a capacitor C, a shorting switch SH, and a read switch R. The eight stages of the network 23 of FIGURE 3 are respectively designated by the numerals 1-8. The sampling switches S are controlled by the DCU control bus 31, the shorting switches SH are controlled by the DCU bus 32, and the read switches R are controlled by the DCU bus 33. Each of the sampling switches S has an input connected at 21 to the output of the LNTA 22. Each of the sampling switches S has an output coupled to its corresponding capacitor C, and each shorting switching SH is connected for selectively shorting the terminals of its corresponding capacitor C. Each read switch R has an input connected to the output of its corresponding sampling switch S, and has an output connected to the IF amplifier 25. The read switches R of stages 1-4 have their outputs coupled to the non-inverting input 35 of the IF amplifier 25, and the read switches R of stages 5-8 have their outputs coupled to the inverting input 36 of the IF amplifier 25. The digital control unit 34 also provides control signals for controlling transistor switches 38 and

39. Switch 38 selectively shorts the terminals of a capacitor coupling the output of the IF amplifier to its non-inverting input 35, and the switch 39 selectively shorts the terminals of a capacitor which couples the output of IF amplifier 25 to its inverting input 36.

The IF amplifier 25 is shown in FIGURES 2 and 3 for illustrative purposes.

5 However, the IF amplifier 25 can be considered as a part of the analog signal processing section 26. In some embodiments, the IF amplifier 25 can be, for example, a continuous time buffer amplifier, a switched capacitor analog baseband filter, or an impedance transformer. The switch and capacitor network 23 includes a high impedance node for sustaining a down-converted information-carrying signal which needs subsequent  
10 processing. The IF amplifier 25 operates to transfer the information to the analog signal processing section 26 with an option to filter it actively or passively while presenting it to section 26.

In some embodiments, the LNTA 22 is AC coupled to the switched capacitor network 23, and in other embodiments, the LNTA is DC coupled to the switched capacitor  
15 network 23. Capacitively coupling the LNTA output to the sampling switches S blocks DC offset build-up which could otherwise occur due to offsets in the LNTA output.

In some embodiments, the shorting switches SH of FIGURE 3 can connect the top plate of the sampling capacitors C to a voltage source. Hence, each switch SH may be used to reset the initial charge on the corresponding sampling capacitor C to a predetermined  
20 value which would be the common mode voltage of the sampling capacitor C as well as the common mode input for the IF amplifier 25.

In some embodiments, the IF amplifier 25 can be used as a buffer, or may itself be a switched capacitor filtering stage which processes the data on the sampling capacitors C while simultaneously presenting that data to the analog signal processing section 26.

In some embodiments, the shorting switches SH can be used to place a common mode voltage in the network 23 while destroying the charges held on the corresponding capacitors C (that is, while resetting the charges on the corresponding capacitors).

Hereinafter, the following nomenclature will be observed. The sampling switch S of a given stage will be designated as S followed by the number of that stage. For example, S1 designates the sampling switch S of stage 1 and S5 designates the sampling switch S of stage 5. Similarly, R1 designates the read switch R of stage 1 and R6 designates the read switch R of stage 6.

FIGURE 3A demonstrates controlling the common mode voltage of one embodiment by resetting the voltage on the sampling capacitors to arbitrary VBIAS before new samples are integrated. Instead of discharging the sampling capacitors after they have been read by the IF amplifier, a predetermined voltage can be placed on them using the shorting switches SH as controlled by the DCU. This feature allows controlling the common mode voltage in this part of the receive chain by the DCU using the SH1-SH8 lines in the embodiment of FIGURE 3A.

FIGURE 4 graphically illustrates a relationship between the local oscillator signals at 29 and the current waveform at 21 in FIGURE 2. As shown in FIGURE 4, the local oscillator signals 29 include a signal LO+ and a signal LO-. The signals LO+ and the LO- can be generated in conventional fashion by the local oscillator of FIGURE 2 in response to

the input voltage waveform 20. The signal LO+ is high during the positive half cycles of the current waveform 21, and is low during the negative half cycles, and the signal LO- is low during the positive half cycles of the current waveform 21 and high during the negative half cycles. Thus, the signal LO+ can be used to sample the positive half cycles of the current waveform, and the signal LO- can be used to sample the negative half cycles of the current waveform.

As shown in the example of FIGURE 4, a first current waveform sample SA1 corresponds to a positive half cycle of the current waveform, a second current waveform sample SA2 corresponds to the immediately following negative half cycle of the current waveform 21, a third current waveform sample SA3 corresponds to the immediately following positive half cycle of the current waveform, etc. Thus, the DCU 34 can gate the signals LO+ and LO- appropriately to the control inputs of the sampling switches S in order to permit the corresponding capacitors C to integrate the portion of the current waveform (positive half cycle or negative half cycle) that is sampled by the associated sampling switch S. The DCU 34 can also gate the signals LO+ and LO- appropriately to operate the read switches R as desired to dump the stored charge from the capacitors C to the IF amplifier 25. In the example of FIGURE 4, the sampling and integrating operations are performed at the Nyquist rate of the RF signal.

FIGURE 5 illustrates in tabular format one example of how the DCU 34 of FIGURE 3 can use signals derived from LO+ and LO- to control the sampling switches and read switches of FIGURE 3. In the example of FIGURE 5, the samples SA1-SA10 correspond to the current waveform 21 as shown in FIGURE 4. The sample SA11 of FIGURE 5 merely

represents the next positive half cycle sample (not shown in FIGURE 4). FIGURE 5 illustrates which sampling and read switches of FIGURE 3 are closed by the DCU 34 during the various sampling intervals illustrated in FIGURE 4. In FIGURE 5 (and also in FIGURES 5A, 6, 6A, 8, 8A, 12, 15A-15B, 17A-17B and 18) the illustrated sampling and read switches are open except during the sampling intervals indicated. The example of FIGURE 5 illustrates sampling and read out at the Nyquist rate of the RF carrier signal. The IF amplifier 25 (see also FIGURE 3) removes the sampled charge from the sampling capacitors C at this rate and subsequently presents it to the analog signal processing section 26.

Referring now to FIGURES 3-5, it can be seen from the example of FIGURE 5 that the positive half cycles of the current waveform are integrated by the capacitors of stages 1-4, and the negative half cycles of the current waveform are integrated by the capacitors of stages 5-8. The integrated positive half cycles are sequentially read out to the non-inverting input 35 of the IF amplifier 25, and the integrated negative half cycles are sequentially read out to the inverting input 36 of the IF amplifier 25. Also in the example of FIGURE 5, the positive and negative half cycles are read out to the IF amplifier alternately, in time-interleaved fashion. This provides full wave rectification. Although not explicitly shown in FIGURE 5, each shorting switch SH can be operated to short the associated capacitor at any time after the charge has been read out via the corresponding read switch R and before the next closing of the corresponding sampling switch S.

The accumulation of charge flowing from the LNTA output into the sampling capacitor for half of the RF period results in direct-conversion to DC. The IF frequency of

the waveform at 35, 36 can be arbitrarily changed by modifying the frequency of the local oscillator (LO) just as in conventional mixers.

Referring to FIGURES 3 and 4, because the capacitors C integrate the current waveform during an entire half cycle thereof for each sample SA1-SA10, any clock jitter in the signals LO+ and LO- (and in gated signals derived therefrom) will tend to have a relatively minor effect on the sample stored in the capacitor, because the integration operation of the capacitor determines the area beneath the waveform in the sampled half cycle. Thus, the current integration operation will typically be affected much less by clock jitter than would a conventional voltage sampling operation. The charge accumulated on a given sampling capacitor during an integration operation is manifested as a voltage on that capacitor, so the analog signal processing section 26 can use well-known conventional discrete time analog signal processing techniques to manipulate the voltages presented by the sampling capacitors.

FIGURE 5A shows another example of timing generated from the DCU which relaxes the operating speed requirements of the IFA. The expression “-do-” in FIGURE 5A and elsewhere means “same as above.” In this example, while four samples are accumulated, four previous samples are read out to the IFA, two combined together on the positive side and two combined together on the negative side. This is an example of “spatial averaging” in which two distinct capacitors (on each side) holding different samples are read together for twice as long. Reading these two capacitors together presents the average of the two to the IFA input which performs a decimation in rate by a factor of two. This can be extended to more than two capacitors on the same side (positive or negative), so more than

two samples can be spatially averaged, with the data rate decimated by the number of capacitors averaged.

FIGURE 6 illustrates in tabular format another example of how the DCU 34 of FIGURE 3 can control the sampling switches S and read switches R. In the example of FIGURE 6, each of the capacitors of stages 1-4 integrates two successive positive half cycles of the current waveform before the capacitor is read out to the IF amplifier, and each of the capacitors of stages 5-8 integrates two successive negative half cycles of the current waveform before being read out to the IF amplifier. Thus, samples SA1 and SA3 are both integrated by the capacitor of stage 1 (via operation of sampling switch S1) before the stored charge is read out (via operation of read switch R1) during samples SA4 and SA5. Similarly, the capacitor of stage 5 integrates the negative half cycles associated with SA2 and SA4 (via operation of sampling switch S5) before being read out (via operation of read switch R5) during samples SA5 and SA6. The shorting switches SH can short the capacitors after they are read out and before they are charged again. In general, a given capacitor can integrate as many samples as desired, but it should be ensured that the charge on the capacitor does not overflow under worst case operating conditions. This includes, for example, ensuring that the largest interferer does not overload the capacitor or the input stage of the IF amplifier.

FIGURE 6 demonstrates an example of a concept referred to herein as “temporal summation.” In FIGURE 6, on each side (positive and negative), two temporally distinct samples are accumulated on the same sampling capacitor before being read out. With the temporal summation illustrated in the example of FIGURE 6, the output rate is decimated in time by a factor of two.

FIGURE 6A demonstrates an example of “temporal summation and spatial averaging” where two temporally distinct samples are accumulated together on each of two sampling capacitors on each side before read out. The decimation factor is now equal to 4 in contrast to the previous examples demonstrating only temporal summation (e.g., FIGURE 6) or spatial averaging (e.g., FIGURE 5A), however the end result is to accumulate the average of four samples. The same end result can be obtained using temporal summation or spatial averaging exclusively (adjusting gain by scaling capacitors).

FIGURE 7 diagrammatically illustrates an exemplary generalized FIR filter function which can be realized by the embodiments of FIGURES 2-4. The generalized FIR filter function of FIGURE 7 includes M taps. A digital sample at time n is multiplied by a coefficient  $cf(0)$ , a sample at time n - 1 is multiplied by a coefficient  $cf(1)$ , a sample at time n - 2 is multiplied by a coefficient  $cf(2)$ , and a sample at time n - M - 1 is multiplied by a coefficient  $cf(M-1)$ . The results of the coefficient multiplications are summed together at 71 and decimated by a factor of M at 72.

FIGURE 8 illustrates in tabular format exemplary operations which can be performed by the DCU 34 of FIGURE 3 to realize the following FIR filter:

$$\frac{1}{2} [x(n)] + \frac{1}{2} [x(n-1)].$$

The coefficients having a value  $\frac{1}{2}$  can be produced by closing two of the sampling switches S during a given sample (e.g. close S1 and S2 during SA1), thereby dividing the current from the LNTA 22 between two capacitors, each receiving  $\frac{1}{2}$  of the sampled current. Then, only one of the two capacitors is read out, thereby providing the desired coefficient value of  $\frac{1}{2}$ . For example, a  $\frac{1}{2}$  coefficient for sample SA1 is realized by closing read switch R2 during



sample SA3 (after both sample switches S1 and S2 were closed during SA1), and a  $\frac{1}{2}$  coefficient for sample SA2 is realized by closing read switch R5 during sample SA3 (after both sample switches S5 and S6 were closed during SA2). As discussed above, switches SH can short their respective capacitors any time between read out (if the capacitor was even read) and the next sample operation. The closing of two read switches simultaneously (e.g. R2 and R5 during SA3) provides decimation by a factor of two in this example. Other FIR filters with any desired coefficients, and any desired number of taps and decimation factor, can be implemented, for example, by providing more than 8 stages and/or varying the number of sampling switches S and read switches R that are closed during each sample. It may be advantageous to close the same number of sampling switches S during each sample, so the LNTA sees a constant load.

FIGURE 8 demonstrates an example of a concept referred to herein as “sliding window” integration. Sliding window integration is an integration technique over multiple time samples. In FIGURE 8, each sample is obtained by integrating the LNTA output on two sampling capacitors, so each individual capacitor has half the voltage due to the two-way current split during integration. This spatial splitting of the sample over two distinct capacitors permits that sample to be used during two distinct read out cycles. In the example of FIGURE 8, the sliding window integration technique sums two temporally distinct samples during any given read out cycle. During the next successive read out cycle, two temporally distinct samples are again summed, but with the time window shifted by one sample, so one of the samples summed in the previous read out cycle is summed again in the next read out cycle. This is illustrated, for example, by noting that sample SA1 is split

between stages 1 and 2, which stages are respectively read out during samples SA2 and SA3; sample SA2 is split between stages 5 and 6, which stages are respectively read out during samples SA3 and SA4; and sample SA3 is split between stages 3 and 4, which stages are respectively read out during samples SA4 and SA5. Using the sliding window integration  
5 technique, read out operations can be performed at the Nyquist rate of the RF carrier, but with temporal summation. The sliding window concept can be extended to longer time summation windows wherein the LNTA output is integrated on any desired number of capacitors, for example all capacitors in each of two or more banks of capacitors (described in more detail below), so that charge corresponding to a given sample can be included in as  
10 many consecutive read out cycles as desired.

The sliding window integration technique can be used to construct a filter with triangular coefficients which place two-zeros on the fold-over frequencies. It is important to realize that summing samples in time is equivalent to decimating the output of a moving average (MA) filter with unity coefficients by a factor equal to the number of accumulated  
15 samples as depicted in FIGURE 7.

Decimation by a factor of M results in folding of the frequency band M-1 times. The transfer function of such a filter before decimation exhibits single zeros at the frequencies which fold over to DC. The intended receiver proposes very low-IF reception or even zero-IF so that the aliasing frequencies fall either very close to (for low-IF) or exactly on the zeros  
20 (for zero-IF) and are rejected by "strategically" placed zeros.

The attenuation by a single zero may not be enough if strong interferences reside at the fold-over frequencies and it is important to increase the rejection of such frequencies by

increasing the number of zeros at these fold-over frequencies. Filters with triangular coefficients place two zeros at these aliasing frequencies and provide a much stronger rejection to them. Such filters can be implemented using the sliding window integration approach. Such a filter can be constructed, for example, using any of the techniques  
 5 described herein that realize fractional coefficients. In some embodiments, a predetermined fraction can be chosen based on the desired coefficient value, and the remaining charge can be discarded. Alternatively, all of the sampled charge can be retained (i.e. do not destroy unwanted charge) while still realizing triangular coefficient filtering.

One exemplary embodiment of a filter realizing the triangular coefficients 1, 3, 3, 1 is  
 10 shown in FIGURE 8B. This structure has twice as many sampling capacitors as shown in FIGURE 3 with the property that the two capacitors of each stage split the total integrating capacitance value  $K$  into fractional values of  $K/4$  and  $3/4 K$ . The read switches  $R1'-R16'$  are used to read out the  $K/4$  samples. A total of eight sampling capacitors are seen by the plus side of the IF amplifier and the same number by the minus side. Four weighted samples are  
 15 accumulated with the ratio 1:3:3:1 and read out and decimated by  $M/2$  instead of  $M$  ( $M=4$  in this case). FIGURE 8A shows the timing for this example.

Note from FIGURE 8A that the read out rate is twice as fast as the rate suggested by reading four accumulated samples, due to the sliding window integration approach. This embodiment shows spatial averaging of 4 weighted samples and provides improved rejection  
 20 to the aliasing frequencies. A time accumulation of weighted samples can also be done by providing appropriate capacitor size to the LNTA in the sampling phase. However, in this approach, the LNTA will see a varying output load.

The above example may also be extended to longer time accumulation on each sampling capacitor shown in FIGURE 8B. Instead of accumulating one sample on one sampling capacitor (realized as two caps which make  $C$  together and can be splitted), we can accumulate an arbitrary number of samples and move to the next capacitor. In this case, one zero will be placed to the fold-over frequencies corresponding to decimation in time on one sampling capacitor. The fold-over frequencies due to spatial averaging with weighted coefficients will see two-zeros and will be rejected by a greater amount.

Referring again to FIGURE 3A, the exemplary embodiments shown therein demonstrate passive infinite impulse response (IIR) filtering obtained by charge sharing the contents of the relevant sampling capacitors (selected by DCU for read operation) with another capacitor  $C_A$ . The read out samples are charge shared with  $C_A$  when the respective sampling capacitors are shorted with  $C_A$ . This splits the total charge on the aggregate of read out capacitors and previous charge on  $C_A$  according to the capacitor ratio of  $C_A$  to the aggregate of read out capacitors.  $C_A$  is never reset, and consequently creates a low-pass filter whose pole is determined by the ratio of the aggregate of sampling capacitors shorted together with  $C_A$  to the value of  $C_A$ . The filtered down-converted signal is transferred by an IFA or a gain block which may also be viewed as an impedance transformer and which presents this data to blocks that perform further analog signal processing.

FIGURE 9 diagrammatically illustrates exemplary dummy stage embodiments which can be alternatively used to generate various fractional coefficients. There are three dummy stages D1, D2 and D3, in the example of FIGURE 9. Each dummy stage includes a sampling switch  $S$ , a capacitor  $C$ , a shorting switch  $SH$ , and a read switch  $R$ . The sampling

switches, shorting switches and read switches are respectively controlled by the DCU busses 31, 32 and 33. By closing the sampling switches S in all of the dummy stages D1-D3, while the sampling switch of one of the stages 1-8 of FIGURE 3 is also closed, the sampled current is divided four ways, thereby permitting realization of a coefficient of 1,  $\frac{3}{4}$ ,  $\frac{1}{2}$ , or  $\frac{1}{4}$ , depending on how many of the capacitors in dummy stages D1-D3 are read when the associated capacitor of stages 1-8 is read. The shorting switches SH of the dummy stages D1-D3 can be activated after the dummy capacitors are read, thereby ensuring that all dummy capacitors (whether read or not) are discharged before the next use of the dummy stages. Note that two sets of the dummy stages shown in FIGURE 9 can be provided, one for cooperation with the stages 1-4 of FIGURE 3 and the other for cooperation with the stages 5-8 of FIGURE 3.

FIGURE 10 diagrammatically illustrates pertinent portions of further exemplary embodiments of a subsampling communication receiver according to the invention. The arrangement of FIGURE 10 is similar to the arrangement of FIGURE 3, except each of the stages of FIGURE 3 is replaced by a plurality of such stages. For example, for  $N = 8$  in FIGURE 10, banks B1, B2, ... BN-1, BN indicate that each of the 8 stages of FIGURE 3 is replaced by a corresponding bank, wherein each bank includes a plurality of stages. Each of the banks receives the current waveform at 21 from the LNTA 22, just as each stage of FIGURE 3 does, and each of the banks also receives control bus inputs from a DCU. Each bank also drives the IF amplifier 25, as does each stage of FIGURE 3.

FIGURE 11 diagrammatically illustrates exemplary embodiments of a bank of stages from FIGURE 10. The example of FIGURE 11 could correspond to any of the banks in

FIGURE 10. The exemplary bank of FIGURE 11 includes 8 stages generally similar to the 8 stages of FIGURE 3, each stage including a capacitor C, a sampling switch S, a shorting switch SH, and a read switch R. The sampling switches S are controlled by a DCU bus 101, the shorting switches SH are controlled by a DCU bus 102, and the read switches R are controlled by a DCU bus 103. Each stage of the bank of FIGURE 11 includes a capacitor  $C_B$ . The value of the capacitor  $C_B$  is determined from the total integrating capacitance value that is selected for the bank. For example, if an integrating capacitance value of K is desired, then the capacitance of  $C_B$  would be  $K/(\text{number of stages in the bank})$ , for example  $K/8$  in FIGURE 11. In this manner, if all of the sampling switches S are closed by DCU 100 during a desired sampling interval, then the desired integrating capacitance K is presented to the current waveform at 21. However, by selectively activating the read switches R, coefficient values of 1,  $N-1/N$ ,  $\dots$   $2/N$  and  $1/N$  can be realized. That is, in the example of FIGURE 11, coefficients of 1,  $7/8$ ,  $3/4$ ,  $5/8$ ,  $1/2$ ,  $3/8$ ,  $1/4$ , and  $1/8$  can be realized. After the desired coefficient has been read out to the IF amplifier, all remaining charges in the capacitors of the bank can be removed by activation of the shorting switches SH. The example of FIGURE 11 can represent any of the banks B1, B2, etc. connected to the non-inverting input 35 of the IF amplifier 25 of FIGURE 10, and can also represent any of the banks BN, BN-1, etc. connected to the inverting input 36 of the IF amplifier 25 of FIGURE 10. In some embodiments, different banks of FIGURE 10 may have different numbers of stages. This advantageously permits various levels of coefficient resolution.

FIGURE 12 illustrates in tabular format exemplary operations which can be performed by the DCU of FIGURE 10, in conjunction with 8 bank structures B1-B8 such as shown in FIGURE 11, to realize the following FIR filter function:

$$\frac{1}{4} [x(n)] + \frac{1}{8} [x(n-1)].$$

5 The leftmost column of FIGURE 12 indicates which sample operation is being performed, in generally the same manner as in FIGURES 5, 6 and 8 above, and the remaining four columns indicate which of 8 exemplary banks (B1-B8) has switches S1-S8 closed, which has switches R1 and R2 closed, which has switch R3 closed, and which has switches SH1-SH8 closed. For each bank, the desired capacitance is used for integration by closing all eight sampling

10 switches S1-S8 during the sampling operation, the coefficient  $\frac{1}{4}$  is produced by thereafter closing read switches R1 and R2, and the coefficient  $\frac{1}{8}$  is produced by thereafter closing read switch R3. Using bank B1 as an example, after the read switch R3 has been closed to produce the coefficient  $\frac{1}{8}$  (during sample SA3), bank B1's shorting switches SH1-SH8 are closed (during SA4) to remove all charges from the capacitors of bank B1. Note, for

15 example, that during sample SA3, the capacitors of bank B2 are integrating the sample SA3, while read switches R1 and R2 of bank B5 are closed to produce the coefficient  $\frac{1}{4}$  for sample SA2, and read switch R3 of bank B1 is closed to produce the coefficient  $\frac{1}{8}$  for sample SA1.

FIGURE 13 diagrammatically illustrates further exemplary embodiments of the

20 banks of FIGURE 10. The bank of FIGURE 13 includes three capacitors, two of which have a capacitance value equal to  $K/4$ , where  $K$  is the desired integrating capacitance, and one of which has a capacitance value of  $K/2$ . The DCU 131 of FIGURE 13 appropriately controls

the sampling switch S, shorting switch SH and the further transistor switches 132-135 such that the current waveform 21 sees the desired capacitance K (by closing switches 132-135 with switch SH open). For read out, the DCU 131 controls the read switch R and the switches 132-135 as desired to produce a coefficient value of 1 (switches 132-135 all closed), a coefficient value of 0.75 (switches 132 and 134 closed, switches 133 and 135 open), or a coefficient value of 0.5 (switches 132-135 all open). After a desired coefficient has been realized using the bank of FIGURE 13, any unwanted charge can be removed by closing switches 132-135 along with shorting switch SH.

FIGUREs 15A-15B illustrate in tabular format exemplary operations which can be performed by stages 1-4 of FIGURE 3 in response to DCU 34. As shown in FIGUREs 15A-15B, beginning at sample SA19, read switch R1 is closed in order to read out the integrated samples stored in the capacitor of stage 1. This read operation of switch R1 continues through sample SA35 and, beginning with sample SA37, the samples integrated and stored by stage 2 are read out by closure of read switch R2. The samples integrated and stored by stages 3 and 4 are thereafter consecutively read out, after which the readout process returns to stage 1 and progresses through stages 1-4 repeatedly. Thus, in the example of FIGUREs 15A-15B, after sample SA17, the integrated samples stored in stages 1-4 are continuously being read out to the IF amplifier 25 (see also FIGURE 3). It should be clear that stages 5-8 can be operated analogously (not shown in FIGUREs 15A-15B) with respect to the even numbered samples SA2, SA4, etc. Under these conditions, there is no opportunity to reset the IF amplifier 25 of FIGURE 3, for example, by operating switches 38 and 39 appropriately to short their associated capacitors.



FIGURE 16 diagrammatically illustrates further exemplary embodiments of the invention which permit resetting the IF amplifier. FIGURE 16 illustrates additional stages such as shown in FIGURE 3, which can be added to the arrangement of FIGURE 3. Stage 9 as illustrated in FIGURE 16 includes a sampling switch S, capacitor C, shorting switch SH and read switch R, just as do the other stages of FIGURE 3. Stage 9, as illustrated, is intended to be cooperable with stages 1-4, and stage 10, as illustrated parenthetically in FIGURE 16, is intended to be cooperable with stages 5-8. The cooperation of stage 9 with stages 1-4 permits resetting of the IF amplifier 25. One example of such cooperation between stages 1-4 of FIGURE 3 and stage 9 of FIGURE 16 is illustrated in FIGURES 17A-17B.

From sample SA1 through sample SA71 in FIGURE 17A, the sampling switch operation of FIGURE 17A is identical to that of FIGURE 15A. However, FIGURE 17A differs from FIGURE 15A beginning at sample SA55, because switch R3 is not closed during samples SA55 through SA71, in contrast to FIGURE 15A. Thus, stage 3 is not read out to the IF amplifier during this period of time, thereby permitting operation of switch 38 to reset the IF amplifier. Stages 5-8 can be operated analogously relative to even numbered samples in generally the same time period to permit operation of switch 39 to reset IF amplifier 25. This creates a period of time during which the IF amplifier can be read and reset. Beginning with sample SA73 and continuing through sample SA121, the sampling switch S9 of stage 9 replaces the sampling switch S3 of stage 3 in the sampling operation. Because the sampling switch S3 of stage 3 is not closed during this period of time, both read switches R3 and R4 of stages 3 and 4 can be closed from SA73 through SA89, instead of

only read switch R4 as in FIGURE 15A. Beginning with sample SA91 and continuing through sample SA125, the read switch operation of FIGURE 17B is the same as the read switch operation of FIGURE 15B. From sample SA127 through sample SA167, the sampling switch operation of FIGURE 17B is the same as shown as in FIGURE 15B.

5 However, beginning with sample SA127 and continuing through sample SA143, no read switch is closed, thereby permitting the IF amplifier to be read and reset. Beginning at sample SA145 and continuing through sample SA161, both read switch R4 and read switch R9 are closed, instead of only read switch R4 as in FIGURE 15B. Thereafter, beginning at sample SA163, read switch R1 is closed, as in FIGURE 15B. Beginning at sample SA163,  
 10 the read switch operation pattern illustrated at SA19 through SA161 repeats itself, and sample switch S9 is again substituted for sample switch S3 in generally the same manner described above. Stages 5-8 can be operated analogously in conjunction with stage 10 to process the even numbered samples.

Thus, by adding stage 9 for cooperation with stages 1-4 and stage 10 for cooperation  
 15 with stages 5-8, additional samples can be integrated and stored while no read switch is closed, thereby permitting the IF amplifier to be reset.

FIGURE 18 illustrates exemplary operations which can be performed by the embodiment of FIGURE 3 to permit resetting of the IF amplifier. In the example of  
 FIGURE 18, stage 1 integrates and stores the first 9 odd numbered (i.e. positive half cycle)  
 20 samples, stage 2 integrates and stores the next 9 samples, stage 3 integrates and stores the next 9 samples, and stage 4 integrates and stores the next 9 samples. This pattern of each stage integrating and storing 9 successive positive half cycle samples is repeated throughout

the example of FIGURE 18. However, in this example, no read switches are closed while sampling switch S4 is closed. After all 4 stages have integrated and stored samples, namely beginning with sample SA73, read switches R2, R3 and R4 are closed along with sampling switch S1, read switches R1, R3 and R4 are closed along with sampling switch S2, and read switches R1, R2 and R4 are closed along with sampling switch S3. Thus, the operation illustrated at sample SA73 through SA143 repeats itself beginning at sample SA145. Stages 5-8 of FIGURE 3 can be operated analogously with respect to the even numbered (negative half cycle) samples. Because no read switches are closed along with sampling switch S4 (and analogously S8), the IF amplifier can be read and reset while stages 4 and 8 are sampling and integrating their allocated number of samples (9 each in this example).

FIGURE 19 is a timing diagram which illustrates exemplary operations which can be performed by stages 1-3 and 5-7 of the arrangement of FIGURE 3. The square wave pulses illustrated in FIGURE 19 are the digital control pulses applied by the DCU to the gates of the sampling switches S of the stages illustrated in FIGURE 19. Thus, for example, stages 1 and 5 are used to integrate samples SA1-SA8, stages 2 and 6 are used to integrate samples SA9-SA16, and stages 3 and 7 are used to integrate samples SA17-SA24. Stages 1 and 5 are then used again to integrate samples SA25-SA32, and so on as illustrated.

Also in FIGURE 19, the term "hold" designates those periods of time wherein both the sampling switch S and the read switch R of a given stage are both open. Also, the term "dump" in FIGURE 19 designates those periods of time wherein the sampling switch S of a given stage is open while the read switch R of that stage is closed, thereby permitting the charge stored in the capacitor C of that stage to be "dumped" to the IF amplifier 25. Thus, as

shown in FIGURE 19, samples SA1-SA8 are dumped from stages 1 and 5 while samples SA9-SA16 are integrated by stages 2 and 6, samples SA9-SA16 are dumped from stages 2 and 6 while samples SA17-SA24 are integrated by stages 3 and 7, and samples SA17-SA24 are dumped from stages 3 and 7 while samples SA25-SA32 are integrated by stages 1 and 5.

5           Thereafter, while stages 2 and 6 integrate samples SA33-SA40, all of stages 1, 3, 5 and 7 are held instead of dumped. Then, while stages 3 and 7 integrate samples SA41-SA48, samples SA25-SA32 (previously integrated by stages 1 and 5) are dumped by stages 1 and 5, and samples SA33-SA40 (previously integrated by stages 2 and 6) are dumped from stages 2 and 6. During the integration of samples SA33-SA40, while samples SA25-SA32 are still  
10           being held in stages 1 and 5, the IF amplifier 25 can be read and reset as illustrated in FIGURE 19. Thereafter, while stages 3 and 7 integrate samples SA41-SA48, stages 1 and 5 “catch up” by dumping samples SA25-SA32 simultaneously with the dumping of samples SA33-SA40 from stages 2 and 6. Thereafter, samples SA49-SA56 are integrated by stages 1 and 5 while stages 3 and 7 dump samples SA41-SA48, after which samples SA49-SA56 are  
15           held in stages 1 and 5 while stages 2 and 6 integrate samples SA57-SA64. This permits the IF amplifier to be read and reset while stages 2 and 6 integrate samples SA57-SA64. Stages 1 and 5 “catch up” while stages 3 and 7 integrate samples SA65-SA72. This “catch up” is again accomplished by dumping stages 1 and 5 (samples SA49-SA56) simultaneously with stages 2 and 6 (samples SA57-SA64).

20           As illustrated by the exemplary embodiments of FIGURES 15-19, various numbers of stages can be utilized and controlled appropriately to permit the IF amplifier to be read and reset with any desired frequency.

Referring again to FIGURE 7, the signal  $y(n)$  can be expressed as follows:

$$y(n) = \sum_{i=0}^{M-1} cf(i) \bullet x(n-i).$$

In the frequency domain, this becomes:

$$Y(z) = C(z)X(z).$$

5 Note that  $C(z)$  can be also be expressed as follows:

$$C(z) = C(z)[(1-z^{-1})/(1-z^{-1})] = C^{diff}(z)/(1-z^{-1}), \text{ where}$$

$$C^{diff}(z) = C(z) - z^{-1}C(z).$$

$C^{diff}$  can be considered to be a filter whose output is given by:

$$Y^{diff}(z) = C^{diff}(z)X(z).$$

10 Note that, in  $C^{diff}$ , the term  $z^{-1}C(z)$  is merely a delayed response of the filter  $C(z)$ , so  $C^{diff}$  is realized by using a filter whose coefficients are obtained by subtracting  $cf(i-1)$  from  $cf(i)$ .

Such coefficients are conventionally referred to as differential coefficients, and the use of filters with such differential coefficients is well known in the art. For a filter having coefficients that are highly correlated, the dynamic range requirement of the filter can be

15 reduced by using the  $C^{diff}$  filter with the differential coefficients. The digital time domain function  $y^{diff}(n)$  corresponding to  $Y^{diff}(z)$  is expressed as follows:

$$y^{diff}(n) = cf(0)x(n) + \sum_{i=1}^{M-1} (cf(i) - cf(i-1))x(n-i) - cf(M-1)x(n-M+1).$$

The dynamic range requirement of a filter utilizing differential coefficients is typically only a small fraction of the dynamic range requirement of the original filter.

20 FIGURE 20 diagrammatically illustrates an exemplary embodiment of a differential filter which can be realized by the embodiments of FIGURES 2-13. The structure of the

differential filter 201 of FIGURE 20 is generally similar to that of the filter illustrated in FIGURE 7 (for  $M=4$ ), except the DCU controls the sampling switches S and read switches R such that the filter utilizes the illustrated differential coefficient values. The differential filter 201 produces the signal  $y^{diff}(n)$ , which is then applied, in the embodiment of FIGURE 20, to an integrating filter 202 which produces the desired signal  $y(n)$ . The integrating filter 202 accounts for the fact that  $C^{diff}(z)$  must be divided by  $(1-z^{-1})$  to obtain the desired transfer function  $C(z)$ . In some exemplary embodiments, the integrating filter illustrated at 202 can be replaced by another recursive filter. In other exemplary embodiments, the filter at 202 can be completely eliminated, and unwanted interferer energy will still be substantially rejected.

FIGURES 21 and 22 diagrammatically illustrate exemplary positioning of a recursive filter (for example the integrator of FIGURE 20 or a lossy integrator) according to the invention. As shown in FIGURE 21, the recursive filter can be implemented within the analog signal processing section 26 of FIGURE 2 and, as shown in FIGURE 22, the recursive filter can be implemented digitally at the digital output side of the A/D converter 27 of FIGURE 2. FIGURES 21 and 22 also illustrate further exemplary embodiments wherein the output of the recursive filter can be applied to a low pass (LP) filter to obtain additional filtering functions. In other embodiments, the low pass filter can be omitted, as shown by a broken line in FIGURES 21 and 22.

The dynamic range of differential coefficients is reduced when using the sliding window integration technique described above relative to FIGURE 8A. This means that a smaller capacitor spread can be used to realize a filter that would otherwise require a much

larger capacitor spread. For example, the original filter may require realizing a capacitor spread of 1 pF – 256 pF, which is very difficult due to large dynamic range. For a narrowband filter, using differential coefficients can advantageously reduce this dynamic range to a much smaller range of variation.

5           FIGURE 23 diagrammatically illustrates exemplary embodiments of portions of the multi-tap digital subsampling receiver architecture of FIGURE 2. FIGURE 23 presents a single-ended example including stages 1-8 as shown in FIGURE 3, but wherein the outputs of all read switches R are connected together at the inverting input of the IF amplifier, whose non-inverting input is connected to a fixed potential (e.g. ground) to provide the single-ended  
10 configuration.

If, for example, stages 1 and 2 are operated to integrate alternate samples in a sequence of J samples, such as shown in the first two rows of the table in FIGURE 24 (see also FIGURE 4), and if the charges stored in stages 1 and 2 are thereafter read out to the IF amplifier 25, as shown (by closure of read switches R1 and R2) in the third and fourth rows  
15 of the table of FIGURE 24, then the equivalent filter is illustrated in FIGURE 25. That is, J consecutive samples, namely SA1-SAJ, are integrated and stored in stages 1 and 2, in response to control signals produced by the DCU on the sampling switch control bus 31. This operation of the sampling switch control bus 31 results in the computation of an inner produce with the sequence {1, 1 ... 1}. Thus, any sampling switch control sequence applied,  
20 for example, to sampling switches S1 and S2 is correlated with the input signal, and the result is stored in the corresponding capacitors of stages 1 and 2. Therefore, despreading of CDMA signals can be obtained by applying the spreading sequence or pseudo-noise (PN)

code at sampling switches S1 and S2. The capacitors of stages 1 and 2 then act as a correlator. The output of the correlator can then be moved to the IF amplifier 25. The DCU can provide the spreading sequence or the PN code at the control inputs of the sampling switches S1 and S2.

5 As shown in FIGURE 24, after samples SA1-SAJ have been integrated by stages 1 and 2, samples SAJ+1-SA2J are sampled and integrated by stages 3 and 4 while the integrated samples from stages 1 and 2 are read out to the IF amplifier. Thereafter, the samples SA2J+1 – SA3J are integrated and stored by stages 1 and 2, while samples SAJ+1 – SA2J stored in stages 3 and 4 are read out to the IF amplifier. Samples SA3J+1 – SA4J (not  
10 explicitly shown) are handled by stages 3 and 4, as stages 1 and 2 continue to alternate with stages 3 and 4, stages 1 and 2 integrating while stages 3 and 4 are reading out, and vice versa.

If the LNTA 22 is designed to provide two independent (e.g. current mirrored) outputs (not explicitly shown in FIGURE 23), with one output connected to stages 1-4 and  
15 the other output connected to stages 5-8, then the structure of FIGURE 23 can parallelize the despread operation, because a different spreading sequence or PN code can be used with respect to stages 5-8 than is used with respect to stages 1-4. This can be viewed as a RAKE operation with stages 1-4 used as a first RAKE finger and stages 5-8 used as a second RAKE finger. The capacitors C associated with each RAKE finger contain the correlator output  
20 values. Thus, stages 5, 6, 7 and 8 process the same samples as stages 1, 2, 3 and 4, respectively, but with a different spreading sequence or PN code.



Continuing with the example of FIGURES 23-25, any additional number of RAKE fingers can be provided by simply adding 4 additional stages for each additional RAKE finger. Moreover, additional stages can also be added for the purpose of relaxing the readout and reset timing of the IF amplifier 25, in generally the same fashion as described above with respect to FIGURES 15-19.

FIGURE 14 illustrates exemplary operations which can be performed by exemplary embodiments of the present invention. At 141, the voltage waveform is transformed into a current waveform. At 142, capacitors are used to integrate samples of the current waveform. At 143, analog signal processing (for example to produce FIR filtering) is performed on the integrated samples.

FIGURE 26 diagrammatically illustrates exemplary embodiments of the invention that can perform I/Q mixing. Two separate (e.g. current mirrored) LNTA outputs are provided. Each LNTA output drives two sampling capacitors, one associated with an input (non-inverting or inverting) of the I phase differential amplifier, and one associated with the corresponding input (non-inverting or inverting) of the Q phase differential amplifier. Examples of the signals ( $V_{ch,I}$  and  $\bar{V}_{ch,I}$  and  $V_{ch,Q}$  and  $\bar{V}_{ch,Q}$ ) that control the sampling capacitors of FIGURE 26 are shown graphically in FIGURE 27. As shown in FIGURE 27, the I phase control signal  $V_{ch,I}$  is in phase with the RF waveform  $V_{RF}$ , and the Q phase control signal  $V_{ch,Q}$  is phase shifted by  $90^\circ$ .

Note that any suitable charge transfer technology can be used to support the exemplary filtering operations described herein. In the exemplary embodiments described

above, voltage is converted to current, which is integrated on sampling capacitors, and the resulting charge is manipulated to perform filtering. However, any technology which permits sampling the area under the RF carrier half periods and then manipulating these samples can be used.

5           It will be apparent to workers in the art that the digitally controlled filtering technique described above can reduce the dynamic range requirements of subsequent stages in the analog front end. By appropriate control of the DCU bus lines, an arbitrary decimating FIR filter function can be realized. Multi-bit coefficient resolution can be obtained in a direct sampling mixer. The invention provides digital controls for an FIR filter, which can be used  
10   to provide a programmable transfer function through a DSP core or other microcontroller/microprocessor. The FIR filter permits rejection of unwanted energy, thereby reducing the dynamic range of subsequent components in the signal path. This has the potential of reducing the power dissipation while providing programmability of the signal path immediately after the LNTA. The invention can be used, for example, to provide a  
15   highly integrated RF front end design in deep submicron CMOS technology at a relatively low cost. The invention is also readily applicable to technologies other than CMOS. The disclosed sampling in the current domain provides a high degree of tolerance of timing jitter in the sampling clock. The invention also provides high linearity in a subsampling receiver architecture because the filter transfer function(s) can be designed to ensure that the sampling  
20   switches can be operated in their linear region of operation during the sampling process.

The invention provides further exemplary advantages, such as the ability to combine charges from different samples to obtain filtering, the ability to mix an RF signal to IF by

controlling the amount of time that the RF waveform is integrated on the sampling capacitor, the ability to mix by commutation (that is, inverting the odd samples and combining them with even samples). Other exemplary advantages include a simple design and robustness.

Although exemplary embodiments of the invention are described above in detail, this  
5 does not limit the scope of the invention, which can be practiced in a variety of embodiments.

FIG. 1 is a block diagram of a system 100 for processing a signal. The system 100 includes an input 102, a processor 104, and an output 106. The input 102 is connected to the processor 104, which is connected to the output 106. The processor 104 is configured to receive a signal from the input 102, process the signal, and output the processed signal to the output 106. The processor 104 may include a microcontroller, a microprocessor, or other suitable processing unit. The input 102 may be a sensor, a transducer, or other suitable input device. The output 106 may be a display, a speaker, or other suitable output device. The system 100 may be implemented in a variety of different configurations, including as a dedicated hardware device, a software program, or a combination of hardware and software.